**What is claimed:**

1. A computer communications system comprising:

a transmit buffer coupled to at least one transmit data line, the transmit buffer adapted to receive data from a host computer and temporarily store the data before transmitting the data over the transmit data line to a physical link of a data network;

a receive buffer coupled to at least one receive data line, the receive buffer adapted to receive data from a physical link of a data network over the receive data line and temporarily store the data before providing the data to a computer; and

an array of communication registers, the array including a data register coupled to the receive buffer, wherein repeated reads from the data register causes data to be read from the receive buffer;

the array further including a status register for storing data identifying a collision of data on the physical link of the data network, the status register readable from the host computer, the status register also including at least one bit signifying an interrupt state in at least one of a read and a write operation.

2. The system of claim 1, further comprising a latch coupled between the array and connections to the data network, the latch storing an error signal identifying an error in receiving a frame of data, the latch retaining the error signal for a period of time sufficient to completely receive the frame of data.

3. The system of claim 1, wherein repeated writes to the data register stores data within the transmit buffer.

4. The system of claim 1, wherein the transmit buffer is coupled to the data network through PHY circuitry.

5. The system of claim 4, wherein the array further comprises a media independent interface register storing at least one signal for controlling operation of the PHY circuitry, wherein signals are passed from the media independent interface register to control the PHY during read and write accesses to the data network.

6. The system of claim 1, wherein the array of communication registers are readable by network communication software executed by a processor of a host computer, wherein data read from the data network is received in frames and wherein the processor analyzes a frame of received data in accordance with frame check data stored within the received frame of data.

7. A computer communications system comprising a media access controller including a receive buffer coupled to receive data from a data network and temporarily store the data before providing the data to a host computer,

the media access controller further including communication registers, the communication registers including a data register coupled to the receive buffer, wherein repeated reads from the data register read data from the receive buffer, and

the communication registers further including a status register adapted to store at least one interrupt bit, the interrupt bit set to indicate the presence of data received from the data network and destined for the host computer, the interrupt bit readable by the host computer to indicate the presence of data to be read.

8. The system of claim 7, wherein the receive buffer is coupled to the data network through PHY circuitry.

9. The system of claim 8, wherein the communication registers include a media independent interface register storing at least one signal for controlling operation of the PHY circuitry, wherein signals from the host computer are passed from the media independent interface register to control the PHY as data are read from the data network.

10. The system of claim 7, wherein the communication registers include a byte-count register storing a value indicative of the number of bytes stored in the receive buffer, the byte count register being decremented as data are read from the receive buffer.

11. The system of claim 10, wherein software resident on the host computer performs a sequence of steps including checking a value stored in the byte-count register and, if the byte-count register stores a non-zero value, reading data from the data register.

12. The system of claim 8, wherein a data transfer through the PHY circuitry sets the interrupt bit and wherein the interrupt bit is read out to the host computer over a data bus of at least one byte of data in width.

13. The system of claim 7, further comprising software operable on the host computer for extracting data from a frame format.

14. The system of claim 8, wherein the status register further includes a plurality of bits settable by the PHY circuitry to identify an error on the data network.

15. The system of claim 14, wherein the plurality of bits includes a carrier sense bit indicative of sensing of a carrier signal at an improper time on the data network.

16. The system of claim 15, wherein the carrier sense bit is directly readable by a MAC program executed within a processor of the host computer.

17. A computer communications system comprising a media access controller including a plurality of communication registers, the communication registers including:

a data register coupled to the receive buffer, wherein repeated reads from the data register reads data received from the data network,

a status register including at least one interrupt bit, the interrupt bit set to indicate the presence of data received from the data network and destined for the host computer, the interrupt bit readable by the host computer,

a media independent interface register storing at least one signal for controlling operation of PHY circuitry coupled to the media access controller, wherein signals from the host computer are passed from the media independent interface register to control PHY circuitry as data are read from the data network, and

a byte-count register storing a value indicative of the number of bytes stored in the media access controller for transfer to the host computer, the byte count register decremented as data are read from the media access controller.